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TECHNOLOGY UTILIZATION

SOLID STATE TECHNOLOGY

A COMPILATION



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Foreword

The National Aeronautics and Space Administration has established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace community. By encouraging multiple application of the results of its research and development, NASA earns for the public an increased return on the investment in aerospace research and development programs.

This publication is one of a series intended to convey such technical information. The Compilation presents a selection of solid state devices as they have been developed, integrated into systems to improve system performance, themselves improved by sophisticated processes and techniques, and, lastly, as they have been studied and shielded within hostile radiation environments.

Additional technical information on individual devices and techniques can be requested by circling the appropriate number on the Reader Service Card included in this Compilation.

Patent Statements reflect the latest information available at the final preparation of this Compilation. For those innovations on which NASA has decided not to apply for a patent, a Patent Statement is not included. Potential users of items described herein should consult the cognizant organization for updated patent information at that time.

Patent information is included with several articles. For the reader's convenience, this information is repeated, along with more recently received information on other items, on the page following the last article in the text.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this Compilation.

Jeffrey T. Hamilton, *Director*
Technology Utilization Office
National Aeronautics and Space Administration

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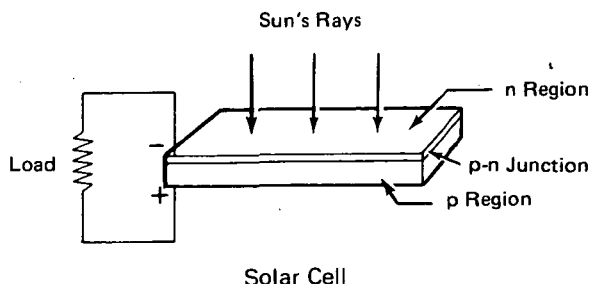
Section 1. Solid State Devices

IMPROVED SILICON SOLAR CELLS

It has been discovered that redistribution of the phosphorus within the n-type layers of n-on-p silicon solar cells results in significant improvements in cell performance. Electrical current output is increased from seven to ten percent, reduction in current output due to radiation damage is substantially lessened, and very shallow junctions are no longer needed.

Redistribution of the phosphorus in the n-type silicon layer is accomplished following initial diffusion of the phosphorus into the silicon wafer. The silicon wafer is simply held at the diffusion temperature for a period of time after the source of the phosphorus is removed. This achieves a reduction in the precipitates present in the phosphorus-diffused region and in the corresponding condition of high silicon lattice strain. Electron micrograph experiments, independent of solar cell studies, have shown the presence of precipitates and, generally, conditions of high lattice strain in phosphorus-diffused regions in silicon. Solar cell experiments have shown a correlation between low current output from diffused regions in silicon and the condition of lattice strain.

As shown in the figure, silicon solar cells consist of a thin layer of n-type (phosphorus-diffused) silicon in contact with a thicker layer of p-type (boron-diffused) silicon. The addition of phosphorus causes the electrical potential of the silicon to decrease when exposed to sunlight; the addition of boron causes the electrical potential to increase when exposed to sunlight. Each photon of sunlight produces a useful current carrier in the silicon. These current carriers diffuse through the silicon to the junction between the two layers; when they cross the junction, they become excess current carriers and thus produce voltage. The n-layer becomes negatively charged, and the p-layer becomes positively charged. However, it has been observed that very little power can be collected from the n-layer. The current carriers produced in this



layer are largely trapped or recombined before they can diffuse to the junction and pass across it. Consequently, n-layers have been made very thin to minimize the distance these current carriers must travel to the junction. By redistributing the phosphorus diffused in the n-layer, more current carriers cross the junction and the current output of the cell is significantly increased. In effect, the distance that the current carriers can diffuse in the silicon before they are lost is increased. Therefore, n-layers can be thicker and the disadvantages of very shallow junctions eliminated. Reduction in current output due to space radiation damage, which also has the effect of reducing current carrier diffusion length, is correspondingly lessened.

The observed increase in short circuit current in diffusion-redistribution silicon solar cells indicates that appropriate design can lead to cells with equally improved total power output. The discovery may also be useful in studying the effects of lattice imperfections on the electrical properties of other materials.

Source: H. E. Kautz
Lewis Research Center
(LEW-10964)

No further documentation is available.

MULTIPORT SEMICONDUCTOR DEVICES

This concerns the design of devices, made of semiconductors, incorporating three or more terminals — multiport devices that transform the signal applied to the input port into a suitable output signal. Semiconductor diodes are limited to applications calling for two-terminal or one-port devices.

The novel device, made of a variety of semiconductors, including amorphous materials, incorporates three or more terminals. Between at least two terminals, switching action occurs as in the double-injection diode or in the "Ovonic" threshold switch. The other terminal pair may perform either another switching function or a control function. The control function arises from either an electric-field effect or a thermal effect or both.

For clarity, assume that the switching diode element (Fig. 1) is a double-injection diode. The top contact is a thin resistive metal film with two

several switching devices; or two or more switching elements could be in such close proximity that they could trigger each other.

The concept is not limited to crystalline semiconductor devices or metallic resistive elements; basically it encompasses all semiconductor switching devices, including amorphous semiconductor components in which threshold voltage is temperature-dependent, and where any thermal element can be incorporated for controlling the threshold voltage.

Moreover, the concept covers devices that return spontaneously to the low-conductance state when voltage is removed, as well as memory-type devices. For the latter, the proper thermal cycling for switching of the device from the low- to the high-conductance state could be independent of the conductance-sensing operation; thus flexibility in design of memory systems would be greatly extended.

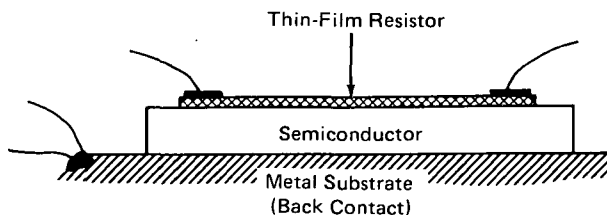


Figure 1. Switching Diode Element; Schematic

terminals between which a potential can be applied. Biasing the diode, below but close to the threshold voltage, puts the diode in the high-resistance state. If a current now passes between the two terminals of the top contact, heat generated adjacent to the active region of the diode lowers the threshold voltage, permitting the device to switch to the low-resistance state.

Very small amounts of power suffice to heat the extremely small volume and cause the switching. In fact, a small amount of control power can switch a greater amount of power. Thus the device provides power gain with the control current applied to a terminal other than that of the current being controlled.

The basic concept can be broadened considerably. For example, the device may incorporate more than one thermally active element; one heater may trigger

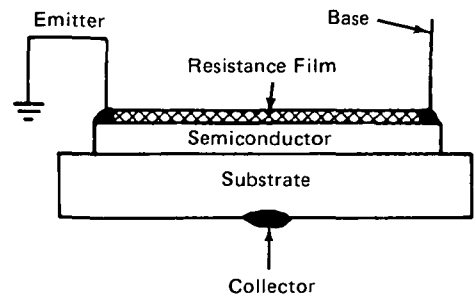


Figure 2. The Terminals Connected to a Transistor Curve Tracer

The validity of the basic concept has been verified with an experimental device (Fig. 2) resembling that shown in Figure 1. One end of the heater was grounded, the other was biased negatively with successively greater values of bias current, and the current-voltage behavior (between the back contact and ground) was plotted for each value of bias current. Although tentative, these results demonstrate that the structures described are readily reduced to practice.

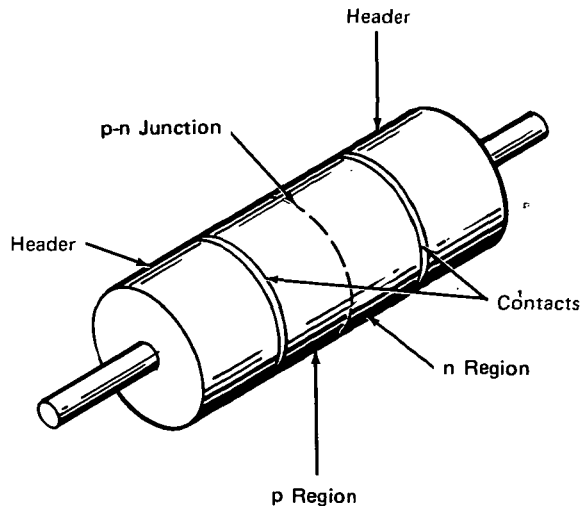
Source: R. Rindner and F. R. Holmstrom of
Electronics Research Center
(ERC-10293)

Circle 1 on Reader Service Card.

SILICON CARBIDE DIODE FOR INCREASED LIGHT OUTPUT

The electroluminescence spectrum of light-emitting diodes made of alpha-silicon carbide generally is confined to the range of 4500 to 6000 angstroms (from the blue to orange regions), with peak intensity occurring at about 5100 to 5200 angstroms (blue-green). A silicon carbide semiconductor device has been developed to improve the overall light output as well as the output in particular regions of the electroluminescent spectrum. The improvement in the electroluminescent behavior of silicon carbide is achieved by the introduction of transition metals, notably titanium, zirconium, or manganese. These impurities (not dopants in the usual sense) introduce levels that can be pumped electrically and affect the efficiency of the recombination process involved in emission of radiation.

The new device comprises a crystal of alpha-silicon carbide having a doped p-type region and a doped n-type region, separated by a p-n junction. The two doped regions are provided with relatively thin non-rectifying contacts, preferably comprising an alloy of gold and titanium. Heavy copper headers are soldered to these contacts. In addition to the dopants that determine the p- and n-type regions, the crystal also contains a selected transition metal. The latter may be present in all or only part of each or both of the p- and n-type regions; but at the very least the transition metal must be in the junction region. Although the junction is illustrated as abrupt, in practice it has a small width (no greater than 0.4 micron). The p-type semiconductivity is achieved by using as a dopant one or a mixture of the Group III elements (e.g., boron, gallium, aluminum). One or more Group V elements (e.g., antimony, arsenic, phosphorus) are included in the crystal to make an n-type semiconductor. The device should have a carrier concentration of at least 10^{15} to 10^{19} atoms per cc. A device is

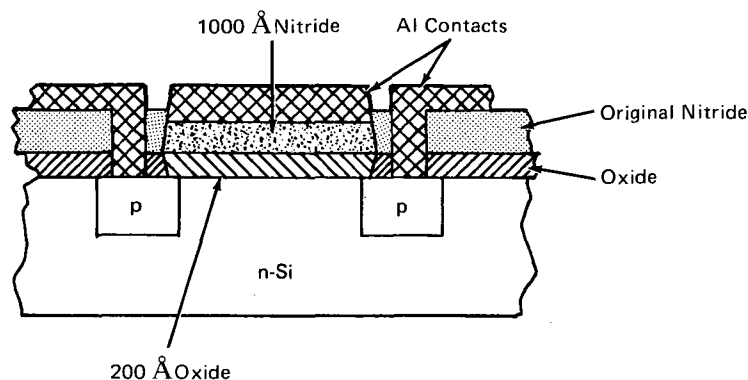


activated to emission by applying a forward bias, as, for example, by connecting the headers to a source of dc of sufficient strength to cause the emission of radiation from the junction region. The exterior surface of the crystal should be polished to optical smoothness and exact perpendicularity to the plane of the junction in order to maximize the light that is emitted radially from the junction region. A convenient process for producing the silicon carbide devices is described in U. S. Patent 3,205,101.

Title to this invention, covered by U. S. Patent No. 3,205,101, has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to Tyco Laboratories, Inc., Bear Hill, Waltham, Massachusetts 02154.

Source: A. I. Mlavsky and L. B. Griffiths of Tyco Laboratories, Inc. under contract to Marshall Space Flight Center (MFS-20063)

RADIATION TOLERANT SILICON NITRIDE INSULATED GATE FIELD EFFECT TRANSISTORS



Metal-Nitride-Semiconductor Field Effect Transistor Structure

MISFET (Metal-Insulated-Semiconductor Field Effect Transistor) devices have been fabricated using a silicon nitride passivation layer on top of a thermally grown thin silicon oxide layer. The addition of the nitride layer has been shown to enhance the radiation tolerance of the MISFET device. This multi-layer dielectric structured device is very attractive in electronic systems which will be exposed to the space radiation environment or to the effects of nuclear weapons. The technology should be of interest to manufacturers of semiconductors and solid state radiation monitoring equipment.

When MIS devices fabricated with the conventional silicon oxide dielectric layer are exposed to an ionizing radiation environment such as that encountered in the Van Allen belts, they have been shown to exhibit a progressive deterioration of the electrical properties. This radiation sensitivity is manifested by a possible shift in the C-V and the I-V characteristics in the direction of higher negative voltages. Therefore, to reach a pre-irradiation drain current level it is necessary to bias the gate more negatively. Under electron irradiation the gate threshold voltage of commercial p-channel devices increases in value from below -5 V to beyond -30 V, depending on operating bias and radiation fluence. This increase requirement will generally make the device inoperative and result in circuit failure.

The two most important physical changes occurring when MIS structures are exposed to ionizing radiation

are (1) the introduction of a fixed positive oxide space charge by the occupation of pre-existing charge-trapping sites in the oxide and (2) the creation of new interface states at the silicon-silicon dioxide interface. The first effect can be greatly reduced by using silicon nitride as the dielectric which has an inherent low trap density and susceptibility to contamination during fabrication. The second effect can be alleviated by in-situ etching before thermal oxidation and prior to heat treatment of the silicon wafer.

The fabrication process variables to be considered are the silicon resistivity type and surface state conditions, the silicon nitride deposition conditions, the contact metallization procedure and the final encapsulation. The actual device, shown in Figure 1, is processed as follows:

The substrate for the device is a 10 ohm-cm, n-type slice of silicon 0.100 ± 0.001 inches thick and mechanically polished on one side. This slice is cleaned, etched and rinsed in deionized water and a silicon nitride layer about 1900 Å thick is then deposited at 900° C by the vapor phase pyrolysis of ammonia and silane.

The windows for the source and drain diffusions are cut into the silicon nitride layer by standard photo-resist etching procedures and boron oxide is then deposited for the p-type source-drain junctions. The insulator material over the gate is removed completely and 200 Å of oxide is thermally grown in the reactor followed by 1000 Å of silicon nitride.

After this, the previously deposited boron is thermally diffused to a depth of 2.5 microns to form the source and drain junctions. Contact windows are then opened over the source and drain and aluminum is evaporated as the contact material. A heat treatment to partially alloy the Al in the source drain regions for lower contact resistance then follows to complete the fabrication process. The devices are individually mounted on four-lead TO-5 headers and subjected to electrical performance and radiation tolerance evaluations.

Documentation is available from:

National Technical Information Service
Springfield, Virginia 22151

Price \$3.00

Reference: TSP69-10253

Source: P. A. Newman
Goddard Space Flight Center
(GSC-10581)

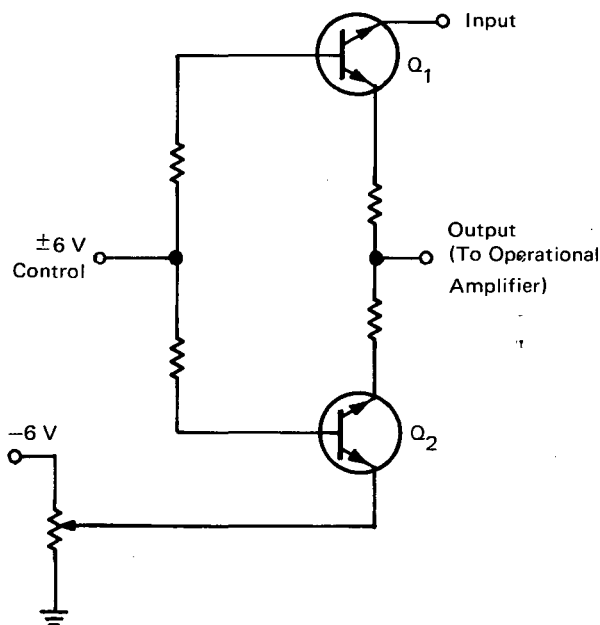
SOLID STATE ZERO-BIAS BILATERAL SWITCH

This circuit was designed to switch a ± 2.5 volt peak, dc to 300 kHz input to an operational amplifier as controlled by a +6 V (*on*) or -6 V (*off*) signal.

The novel feature of this circuit is the use of the bilateral transistor Q_2 which draws a saturation current of equal amplitude and opposite direction to the saturation current of the bilateral transistor Q_1 . As a result, the dc bias effect is canceled at the output (input summing point of the operational amplifier). Since Q_2 is switched *on* when Q_1 is *on*, and *off* when Q_1 is *off*, the operational amplifier has a true zero dc bias in both signal *off* and signal *on* conditions.

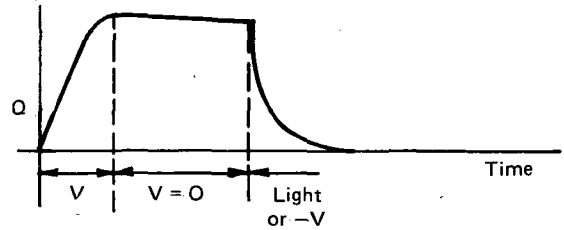
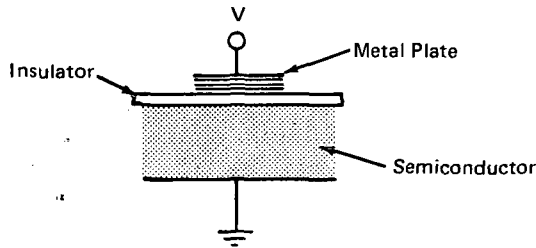
This switching should be useful in a wide variety of signal switching and control circuits.

Source: J. M. Husted of
RCA Corp.
under contract to
Goddard Space Flight Center
(GSC-532)



Circle 2 on Reader Service Card.

IMPROVED SOLID STATE ELECTRON-CHARGE-STORAGE DEVICE



This simple solid state charge-storage device should find application in memory systems and in high-resolution arrays for light-responsive image sensing. The device can be fabricated without the use of diffusion techniques and offers high yield in multiple arrays. It allows charge release with light striking only the edge of a metal electrode, without penetrating to the interface of an insulator. This unique property simplifies electrical contacting. The device is charged by applying a voltage pulse, and discharged by exposure to light or by a voltage pulse of opposite polarity.

As shown in the sketch, the storage device consists of a semiconductor (e.g., n-type silicon) and a metal plate, with an insulator sandwiched between the two components. The semiconductor must have suitable electronic states on its surface, and the insulator must be thin and of high resistivity. When positive charging voltage, V , is applied to the sandwich, electrons are drawn to the surface of the n-type silicon (an opposite argument may be used for the p-type silicon) and the semiconductor surface states acquire

a charge Q . After the charging voltage is turned off ($V = 0$), the surface states retain their electrons. These electrons are in a metastable state and will discharge when exposed to light or when a suitable $-V$ pulse is applied. Discharge of the unit can be sensed by measuring the current in an external circuit; the current is determined by the amount of charge stored during the application of charging voltage.

The following documentation may be obtained from:
National Technical Information Service
Springfield, Virginia 22151
Single document price \$6.00
(or microfiche \$0.95)

Reference:

NASA CR-90046 (N68-10098), Impurities and Interface States in the SiO_2/Si System.

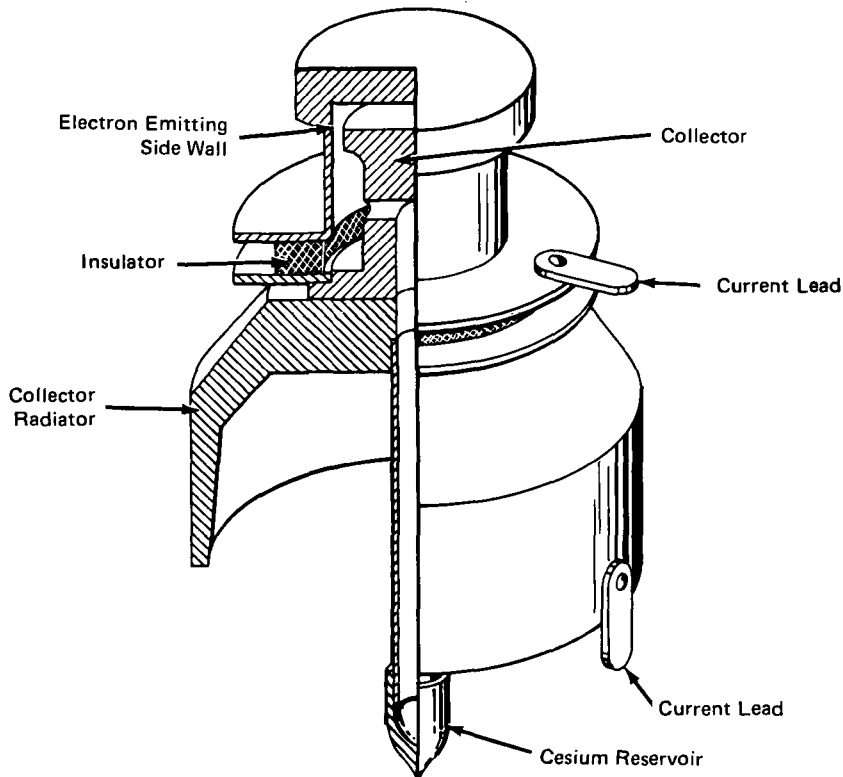
Source: A. B. Kuper of
Case Western Reserve University
under contract to
NASA Headquarters
(HQN-10152)

THERMIONIC DIODE SWITCHING HAS HIGH TEMPERATURE APPLICATIONS

Solid-state switches are currently being used to "chop" the output from low-voltage/high-current power sources. Temperature limitations and radiation damage susceptibility of semiconductor switches severely limit their application to high temperature or radioactive power source conditioning. To overcome these difficulties, the semiconductor switch must be placed in a remote location; however, excessive system degradation results from line losses.

This thermionic diode switch permits "chopping" in the immediate vicinity of the power source, regardless of the adverse environment.

When operated under low emitter temperature (1273 K) and low cesium reservoir temperature (< 473 K) conditions; the thermionic diode exhibits dual mode (plasma mode and unignited mode) properties of immediate application to high current switching. In this temperature region the thermionic



diode has lost its power generation capability; however, it has developed characteristics required of a current switch. In what has been referred to as the plasma mode, the thermionic diode will pass current densities in excess of 12 amp/cm^2 with a forward voltage drop less than 0.6 volts. When the diode is switched out of the plasma mode into the conventional unignited mode, voltages up to 4.0 volts may exist across the diode with only milliamperes of current flowing through it. Thus, by placing a thermionic diode in series with a low-voltage (< 4.0 volts)/high-

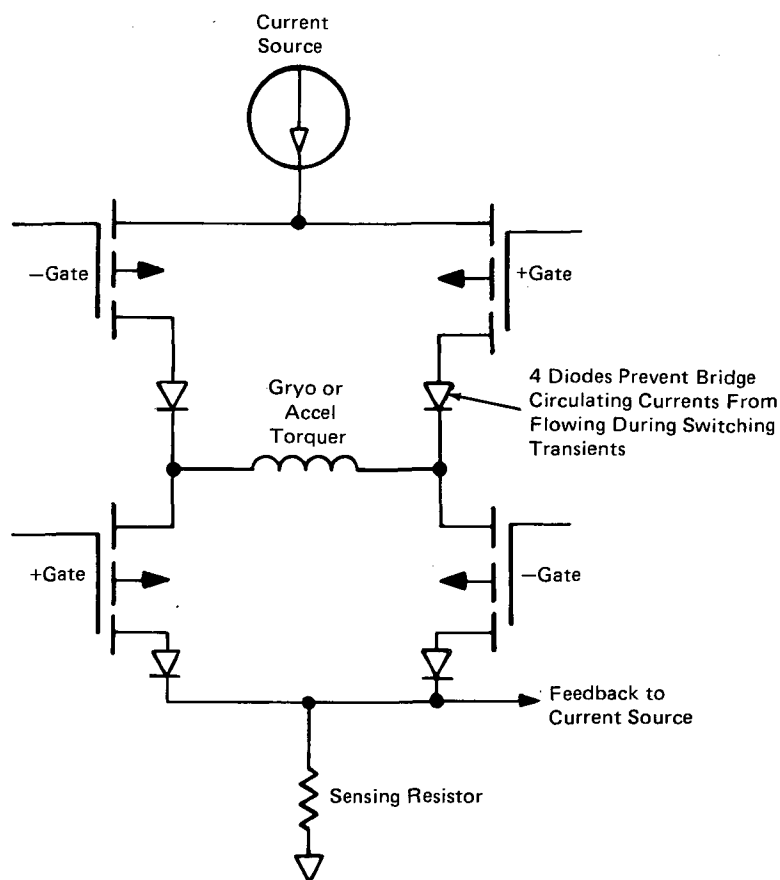
current power source, the output of the source may be chopped by alternately pulsing the thermionic diode switch into the plasma and extinguish modes. The above figure shows the diode geometry successfully tested.

Source: K. Shimada and S. S. Luebbers of Caltech/JPL under contract to NASA Pasadena Office (NPO-10404)

Circle 3 on Reader Service Card.

Section 2. Systems Employing Solid State Devices

TORQUE BRIDGE FOR "LAGLESS" CONTROL-LOOP RESPONSE



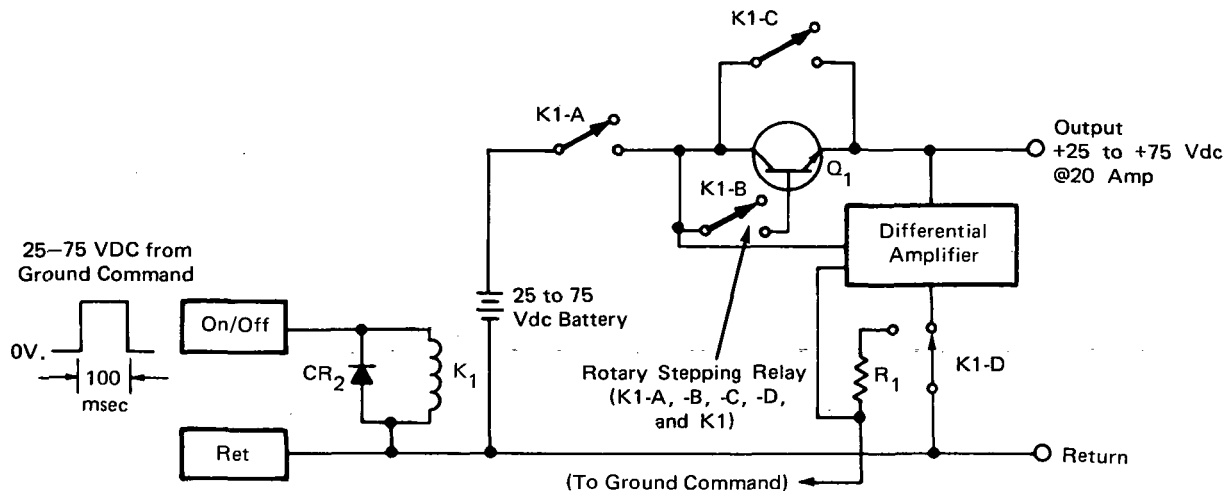
This is a novel solid state logic gate, consisting of four diode-shunted metal oxide semiconductor field effect transistors (MOSFET's), which is coupled to the sensing coil of a gyroscope. The device, which uses current differentiation to achieve "lagless" control loop response should interest manufacturers of electromechanical control equipment. It appears particularly well suited for adaptation to the automatic torque control systems employed in automotive transmissions, and in crane and hoist motor controls. The new torquing bridge is shown schematically

in the figure. Its simple design results in a lower than usual total gate leakage, permitting operation with lower than usual bias currents. This results in better loop performance where temperature is a function of gate leakage.

Source: L. W. Newberry, Jr., of
Honeywell, Inc.
under contract to
Johnson Space Center
(MSC-13853)

No further documentation is available.

HYBRID SOLID STATE SWITCH REPLACES MOTOR-DRIVEN POWER SWITCH



Note: All contacts are shown in the off position.

Presently available motor driven switches used on spacecraft are heavy, large, produce a stray external field, and are costly.

This innovation is a hybrid solid state switch that uses both a transistor circuit and relay contacts. The transistor circuit handles the turn-on and turn-off transients and allows only 3 volts or less to appear across an associated pair of relay contacts during contact transfer. By limiting the open circuit voltage during transfer, unusually high transient currents at reasonable cycle life can be handled by a small relay contact. After transfer, the open circuit voltage may be increased, as this is only limited by the contact insulation.

A transistor circuit handles the closing and opening transients and limits to 3 volts or less the voltage appearing across an associated pair of relay contacts during contact transfer. The relay contacts are closed for the steady state load and provide a minimum voltage drop.

To eliminate battery current drain, the associated logic circuitry is completely disconnected during the steady state on or off periods. Ground (or remote) hard line commands bring this circuitry into action only during transfer. A single rotary stepping relay using rolling contacts is employed to accomplish the switching. It is the electrical equivalent of a 4-pole mechanical latching relay. The relay has

provisions for make-before-break and make-after-break contact arrangements and is capable of performing certain time dependent logic functions, which are primarily of a switching nature.

To reduce weight, much of the logic circuitry is located at the remote command position. A differential amplifier measures the voltage that appears across the switch contacts that are to handle the full load current. When 3 volts or less appear across these contacts, a signal is sent to the remote logic to step the relay which will close the contacts. On opening, the circuitry maintains a maximum of 3 volts across the load current carrying contacts until the contacts are fully open. The voltage may then rise to its full open circuit value.

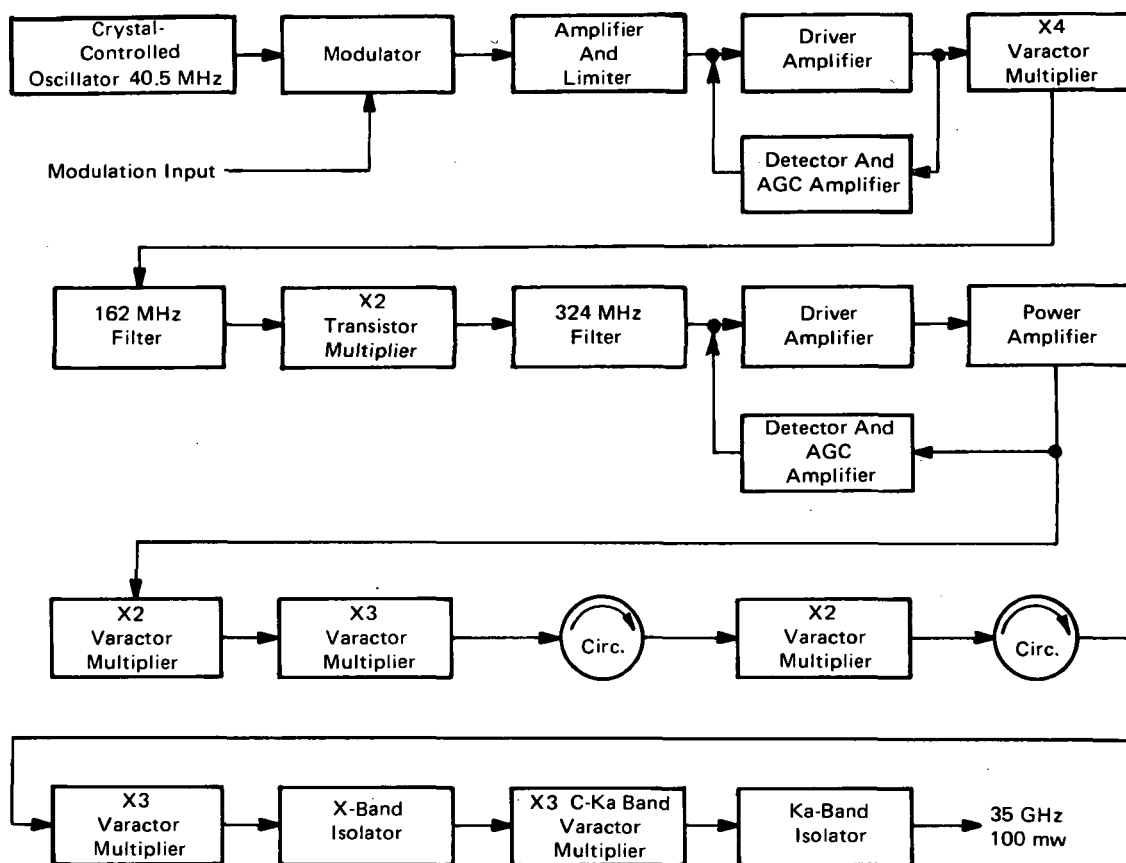
The hybrid solid state switch has been breadboarded and satisfactory test results have been obtained at -10° , 25° , and 75° C.

This switch could be used for high-current switching at high voltages using small relay contacts where a compact, lightweight, reliable switching device is needed. It could be used, for example, for heavy duty motors where large starting currents are required to drive the pumps of washing machines and oil burners.

Source: A. I. Schloss and R. A. Booth
Jet Propulsion Laboratory
(JPL-931)

Circle 4 on Reader Service Card.

A 35-GHz SOLID STATE TRANSMITTER/DRIVER



A solid state transmitter/driver (multiplier) signal source has been designed and fabricated to produce a stable crystal-controlled CW power output of 100 mw at 35 GHz. The circuit requires 60 watts of dc input power and exhibits a signal/noise ratio of at least 30 dB below the carrier at 35 GHz. The signal source is contained in a package measuring 20 x 25 x 14 cm (8 x 10 x 5.5 inches) and weighing approximately 8 kg (18 pounds).

It includes a series of semiconductor amplifiers and multipliers which produce a stable crystal-controlled drive power of approximately 18 watts at 325 MHz. This drive is then applied to a chain of varactor multipliers to a frequency of 35 GHz. The total frequency multiplication factor is 864. Printed-circuit, coaxial, stripline, and waveguide techniques are used for the various amplifiers and multipliers. A phase-modulation exciter is included in the source for telemetry signals.

As shown in the block diagram, the multiplier chain starts with a crystal-controlled oscillator operating at 40.5 MHz. A bandpass filter of 0.02% bandwidth is provided within the oscillator module to limit the noise bandwidth. Following the oscillator, a phase modulator is incorporated to allow frequency modulation of the output. The frequency response of the modulator is 400 Hz to 100 kHz, and it will produce a maximum deviation of ± 215 kHz from 35 GHz output frequency. A limiter-amplifier follows the modulator to remove any amplitude modulation produced in the modulator. An AGC drive amplifier is then used to drive an X4 varactor multiplier to produce a stable 20 mw output at 162 MHz. An m-derived bandpass filter is then employed to suppress the third and fifth harmonics of 40.5 MHz created by the X4 multiplier. Adequate suppression of the spurious harmonics is especially important in the lower end of the chain, since amplification of these

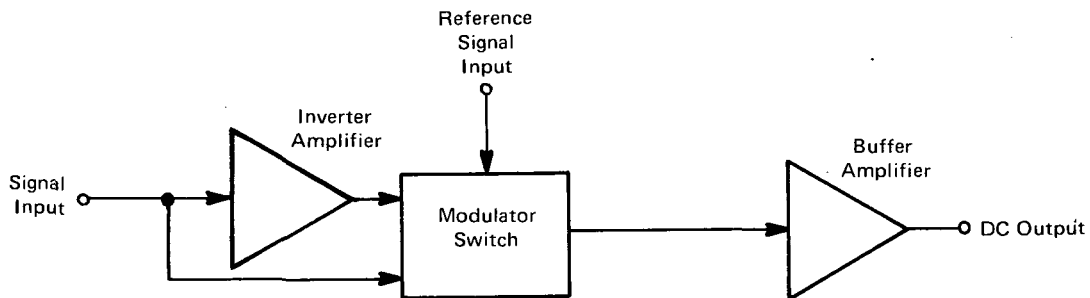
(spurious enhancement) is a function of the square of the multiplication factor of the multiplier chain. A transistor doubler is employed to multiply the frequency to 324 MHz and is followed by a 2-section bandpass filter for additional harmonic suppression. The resulting 324 MHz, 100 mw signal is then amplified to 18 watts by a linear driver and power amplifier string. An AGC loop around this amplifier insures a constant drive to the following multiplier regardless of temperature variations. Following the power amplifier, two lumped element varactor multipliers, a doubler and a tripler, are used to multiply the frequency to 1.95 GHz. A stripline circulator is used to isolate these multipliers from the following stripline S-C band doubler/circulator module. The output of this module is 3.9 GHz at 1.7 watts. A transition to Ku band waveguide is accomplished in the following C-X band tripler. The output of this unit is over 500 mw at 11.7 GHz. A waveguide isolator is used between this multiplier and the final multiplier in the

chain. This final multiplication from 11.7 GHz to 35 GHz is accomplished by a cavity type tripler which provides 125 mw output power. With the inclusion of a final waveguide isolator and the output waveguide, a power output of 100 mw at 35 GHz is available at the output of the unit. Under normal operating conditions, the source will consume 60 watts of primary power from an unregulated 36 VDC supply in the booster. A regulator circuit has been incorporated in the unit to provide the stable 28 VDC power source required for operation of the multiplier chain.

Source: X. A. De Angelis of
Sylvania Electric Products Inc.
under contract to
Marshall Space Flight Center
(MFS-20152)

Circle 5 on Reader Service Card.

SOLID STATE PHASE DETECTOR REPLACES BULKY TRANSFORMER CIRCUIT



This is a miniature phase detector used in a phase lock loop associated with a sub-bit detector in an integrated data-link circuit. The phase detector is used in lieu of a bulky transformer circuit commonly incorporated in phase lock loops. Input requirements are compatible with standard logic levels.

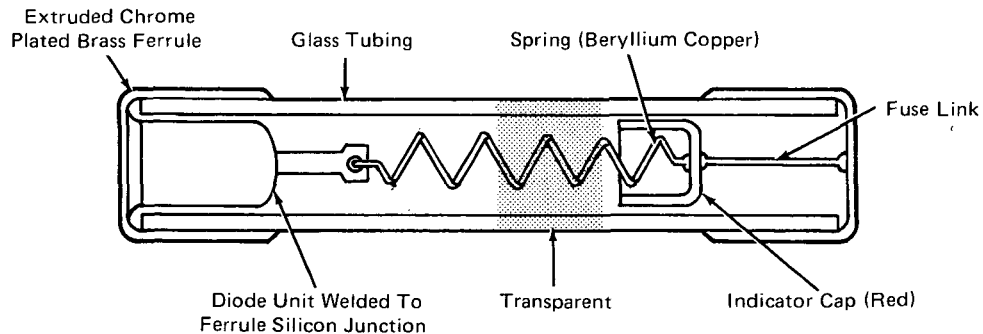
The solid state phase detector employs MOSFET's (Metal Oxide Semiconductor Field Effect Transistors). The detector consists of an inverter amplifier, a modulator switch, and a buffer amplifier. The output of the inverter amplifier is a signal that is inverted (180 degrees out of phase) with respect to the

input signal. The modulator switch performs a mixing function. It provides a signal of fixed amplitude but opposite polarity every half cycle at a rate determined by the reference switching frequency. This switching function is accomplished by two MOSFET's (in the modulator switch), one of which is connected to the input signal and the other to the inverted signal.

Source: C. L. Moberly of
Motorola Inc.
under contract to
Johnson Space Center
(MSC-11007)

Circle 6 on Reader Service Card.

FUSED DIODE PROVIDES VISUAL INDICATION OF FUSE CONDITION



An electrical component has been designed that combines a circuit protective fuse and a semiconductor diode within a single transparent cartridge. The component also provides means for visual indication of fuse condition to preclude the necessity of making resistance checks with an ohmmeter. This is of particular value where many fused diodes are used in a given system that must be periodically checked.

The fused diode consists of an elongated tube fabricated from a transparent heat-resistive material. The ends of the tube are closed with electrically conductive end caps, and layers of opaque material coat the interior for approximately one-third the length of the tube from each end. A diode is secured to one end cap, and a fuse, with a spring and indicator cap providing an electrical connection between the two elements, is secured to the other

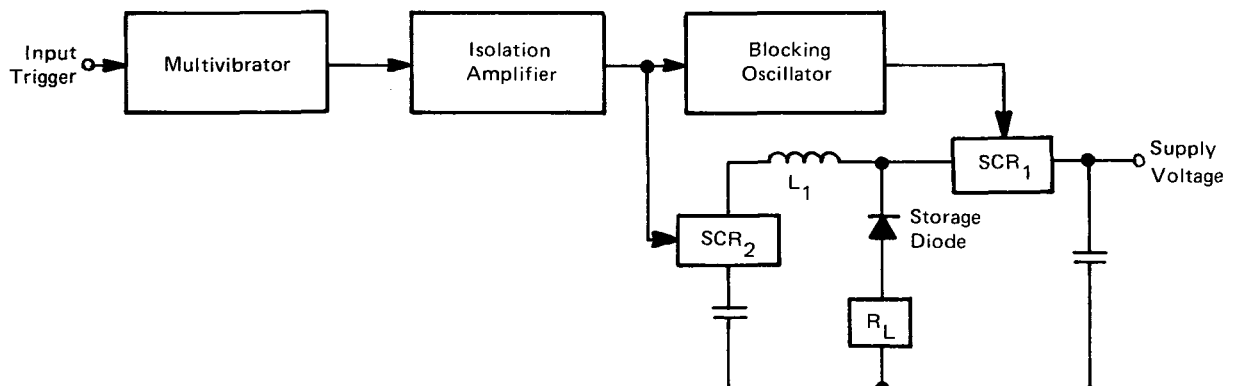
end. The spring serves to bias the indicator cap so that, should the fuse wire melt due to an excess of current, the indicator cap will be displayed in the transparent portion of the tube.

The fused diode may be used wherever a need exists for circuit protection from the shorting of a specific component as opposed to protection from a short at any point within the circuit. It may be used in many applications where relay actuation requires arcing noise suppression. This device would be beneficial in multiple applications where a quick visual inspection of the fused diode could be performed instead of making the more time consuming ohmmeter checks on each diode to determine condition.

Source: K. H. Jenkins
Kennedy Space Center
(KSC-67-16)

Circle 7 on Reader Service Card.

LABORATORY PULSE MODULATOR USES MINORITY CARRIER STORAGE DIODES



Solid-state modulators producing high peak power have been generally limited to those employing either magnetic compression techniques or pulse forming networks and are usually restricted to operation at a single pulse width and pulse repetition rate.

This pulse modulator is capable of continuously variable pulse widths over a 10 to 1 range of 1.0 microsecond to 0.1 microsecond and operation over a wide range of pulse repetition rates. Pulse width diversity is obtained by operating step-recovery diodes in the reverse conduction mode.

The block diagram illustrates the various stages used in the storage diode modulator. The first stage is a multivibrator turned on by a 3.5 volt, 1 microsecond system input trigger. The multivibrator output pulse, variable in width from 5 to 50 microseconds, is coupled to an emitter-follower type isolation amplifier whose output is directly coupled to SCR₂ that controls the charging current for the storage diode.

The amplitude level of the gate trigger is approximately 5 volts, or about twice the minimum amplitude required. A second output from the isolation amplifier is inverted, differentiated, and used to trigger a blocking oscillator whose output is coincident with the multivibrator output trailing edge. Collector-base feed design of the blocking oscillator allows heavy loading without suppression regeneration. The output winding of the blocking oscillator is referenced to the cathode of the main discharge switch SCR₁ which provides the reverse storage diode current (load current). The gate output to SCR₁ is 10 volts to assure rapid turn on.

Source: Sylvania Electronic Systems
under contract to
Marshall Space Flight Center
(MFS-2442)

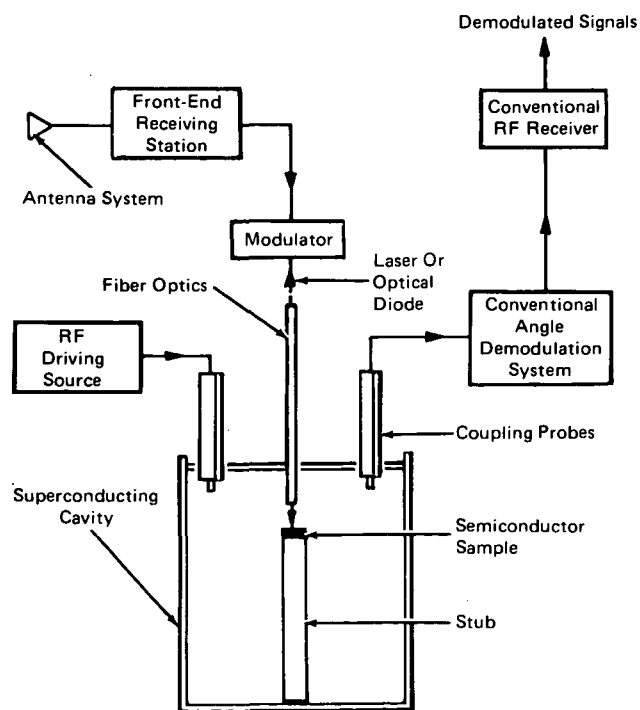
Circle 8 on Reader Service Card.

RF NOISE SUPPRESSION USING THE PHOTODIELECTRIC EFFECT IN SEMICONDUCTORS

A technique using the photodielectric effect of a semiconductor in a high-Q superconductive cavity has been developed which gives an initial improvement of 2–4 dB in the signal-to-noise enhancement of conventional RF communication systems. This technique may readily be applied in conjunction with existing ground receiving station equipment and is of considerable interest to those involved in advanced communications systems.

The capabilities of spacecraft-to-ground communication systems are limited by the relatively low transmitter powers available and by the vast distances over which the signals travel. To increase the detection capabilities of the receiving station, large parabolic antennas 26 m or 64 m (85-foot or 210-foot) and complex low-noise receiving systems (traveling-wave masers) are required.

A system has been conceived in which a wide-band signal plus noise can be transmitted through a narrow-band cavity due to parametric perturbation of the cavity frequency or phase. The tunable beat-frequency cavity acts as a narrow-band tracking filter and suppresses noise outside of its bandpass. Initial test results show a 2–4 dB improvement in output signal-to-noise enhancement, with further improvement



possible through the use of higher Q cavities and a more optimum selection of semiconductor specimens.

The rf signal, received through the antenna system and mixed down to a suitable frequency, modulates an optical diode. Background (thermal) noise in the form of a white gaussian process is present throughout the entire signal bandwidth. The emitted light from the diode is directed via a fiber optic bundle to a high purity semiconductor which terminates a $\lambda/4$ stub in a resonant cavity. The cavity's surface is made superconducting to ensure a high cavity Q. The modulated light beam is absorbed in the semiconductor and excess electron-hole pairs are created from the light photons. These free carriers change the real part of the complex dielectric constant

of the semiconductor which in turn changes the resonant frequency of the cavity. It can be shown that the resonant frequency change is in proportion to the light induced change of the dielectric constant. Thus, the signal modulation present on the light beam is impressed upon the instantaneous cavity frequency as a perturbation. The cavity tracks the instantaneous signal modulation and rejects the thermal noise outside the passband of the cavity. Conventional electronics are then used to recover the signal.

Source: G. D. Arndt
Johnson Space Center
(MSC-12259)

No further documentation is available.

SOLID STATE VARIABLE TIME DELAY

This device is designed for use in electronic circuits wherever a fast reacting variable time delay is required, and should prove valuable for application in the communications industry, and to technical personnel involved in the design and development of microwave components and systems. The solid state variable time delay line offers the following advantages: (1) is inexpensive and space saving, eliminating the need for extra equipment to utilize the delay time; (2) does not require mechanically moving components, eliminating vibrations which could prove detrimental in a sensitive environment; (3) does not require the use of a magnetic field to control a time delay; and (4) features the capability for both amplifying and delaying a signal.

Fixed and variable delay lines are widely used in microwave electronic circuits and systems. However, the fixed lines have had the disadvantages of being expensive and limited in scope. Some solid state variable time delay lines have been developed, but they rely primarily on a mechanical means for changing the delay of the delay line. Recently, variable time delays have been designed using the magnetoelastic properties of certain materials such as YIG (yttrium-iron-garnet). The major disadvantage of these materials is that they require a magnetic field, which may be undesirable in specific environments.

Using cadmium sulfide (Figure 1) as the piezoelectric material, the magnitude of the voltage had no effect on velocity. In Figure 2, with gallium arsenide

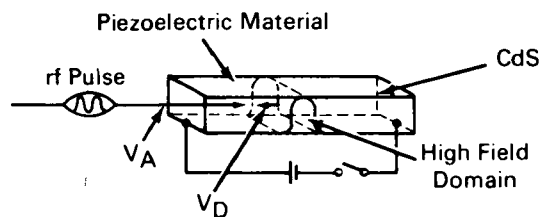


Figure 1

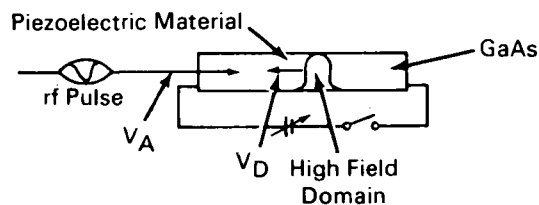


Figure 2

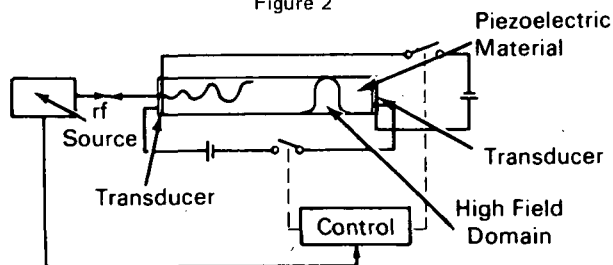


Figure 3

as the piezoelectric material (similar materials will serve), the velocity of movement of the high field domain can be varied by controlling the magnitude of the dc voltage creating the high field domain, thus offering an additional method of control.

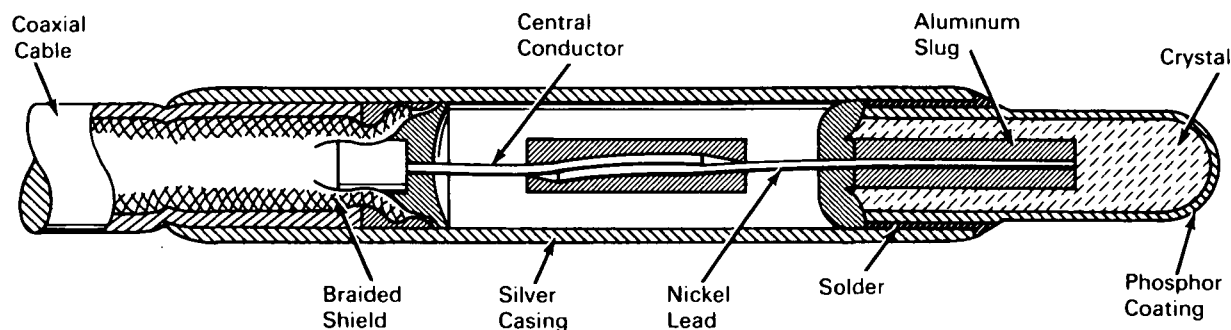
An electric source is applied across the ends of the crystal (Fig. 1). A high field domain then propagates from the negative to the positive end of the material (in the V_D direction). A transducer adapted to receive an rf pulse is mounted on the positive end of the piezoelectric material. When an rf pulse is applied to the transducer, an acoustic wave is generated that propagates through the material toward the high field domain (in the V_A direction). The acoustic wave is then reflected because the elastic properties of the high field domain and the bulk of the material differ. The reflected signal propagates back through the material to the transducer and from the transducer out of the material. The total time delay is the time it takes for the acoustic wave to travel from the transducer to the high field domain and back to the transducer. By varying the point of interaction between the high field domain and the acoustic wave, the total

time delay can be varied. The point is controlled by varying the time of creation of the high field domain relative to the time of application of the rf pulse. The variation in application time is determined by the nature of the piezoelectric material. In some devices, the transducer can be eliminated because certain piezoelectric materials form their own transducers. Figure 3 shows how the acoustic wave is amplified as well as delayed. It also illustrates a means for controlling time of application of various voltages to the body of piezoelectric material, thus providing variable time delay and degree of amplification.

Source: T. M. Fitzgerald
Electronics Research Center
(ERC-10032)

Circle 9 on Reader Service Card.

SEMICONDUCTOR FORMS BIOMEDICAL RADIATION PROBE



This is a reliable miniaturized radiation dosimeter for biomedical application *in vivo*. External dosimeters do not accurately indicate dose level within the irradiated cells because the greater radiation damage is caused by photoelectrons and knock-on protons. Proposed chemical dosimeters for *in vivo* applications are only partially satisfactory since they will not indicate rate of absorption or number of particles absorbed.

This semiconductor radiation detector is in the form of a slender probe that is easily inserted into body tissue. The probe has a signal to noise ratio that

is acceptable to recording equipment and it provides realistic measurements of the spatial and energy distributions of radiant electrons and protons.

The probe detecting element is a semiconductor diode of the junction type, fabricated from a high resistivity silicon crystal doped with p-type impurities. The probe has the general shape of a clinical thermometer with the detector in the form of the mercury reservoir. The p-n type junction at the crystal is formed by the diffusion of phosphorus over the crystal surface. A silver casing holds the phosphorus coated crystal and connects with the ground lead

(braided shield) of a miniature coaxial cable whose central conductor contacts a nickel lead from an aluminum slug in the body of the crystal. The silver casing is tin soldered to the phosphorus coated crystal by means of a nickel plate on the phosphorus and the other end is hermetically sealed to the coaxial cable external insulation which is impervious to body fluids.

In operation, reverse bias is applied to the P-N junction, and radiation penetrating the junction is converted to voltage pulses that are conducted to recording equipment via the coaxial cable.

This device would be useful in evaluating blood flow problems by insertion into veins and arteries to measure the spatial and energy distributions of radioactive tracers.

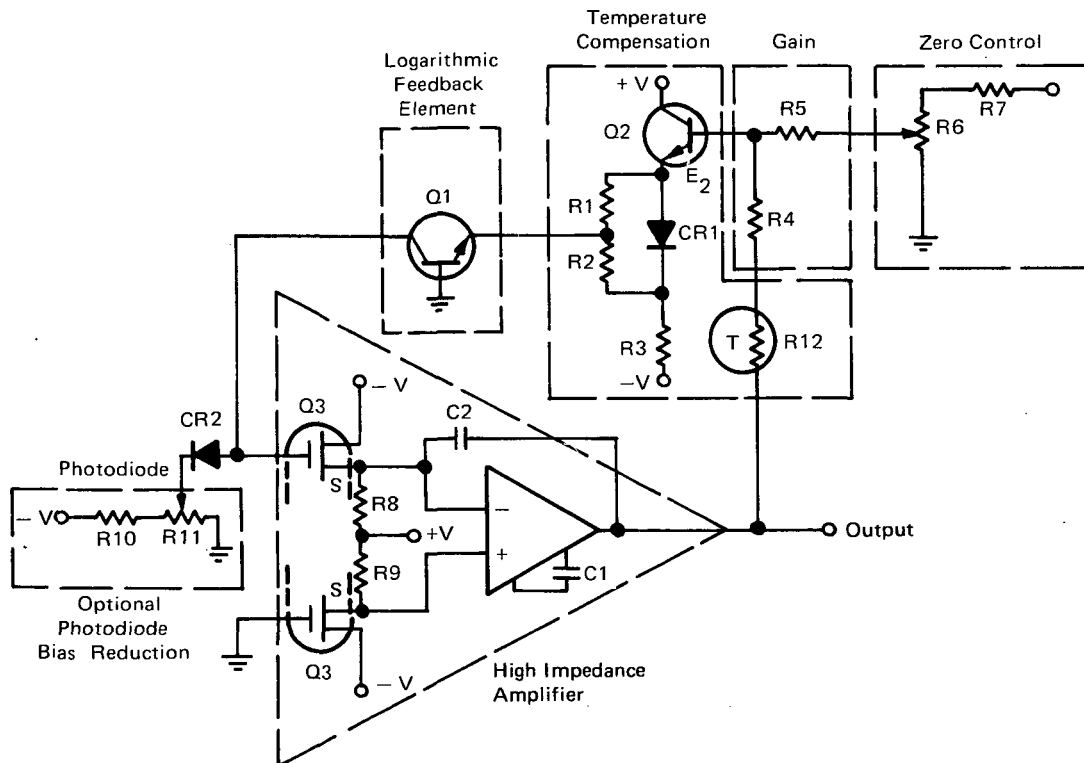
This invention has been patented by NASA (U.S. Patent No. 3,427,454). Inquiries concerning non-exclusive or exclusive license for its commercial development should be addressed to: Patent Counsel, Mail Code AM, Lyndon B. Johnson Space Center, Houston, Texas 77058.

U. S. Patent No. 3,427,454 may be obtained from the United States Patent Office, Washington, D. C. 20231. Price \$0.50.

Source: F. P. Burns and J. E. Friedericks of Solid State Radiation, Inc. under contract to Johnson Space Center (MSC-320)

Circle 10 on Reader Service Card.

SOLID STATE LOGARITHMIC RADIOMETER



A very small, lightweight, temperature-compensated radiometer, with no moving parts, detects spectral intensities encompassing more than five decades over a range of at least 300 to 800 nanometers at power levels as low as 10^{-6} W/cm².

A combination of temperature-compensated logarithmic amplifiers and specially prepared PIN photodiodes operate in a zero-bias mode.

The PIN photodiode used as the sensor for the radiometer is biased at a constant, low voltage to provide an output current that bears a linear relationship to the incident radiation and is relatively free of distortion, independent of environmental conditions, and has low 1/f noise. Operation at bias levels near zero voltage also provides a low effective dark current, and permits the use of simple circuitry to compensate for the effects of temperature. However, this mode of operation leads to an increase in noise current, a decrease in quantum efficiency by a few percent, and a factor of five reduction in speed.

The amplifier used in connection with the PIN photodiode consists of a high-gain, integrated circuit, operational amplifier with a high-impedance matched-pair MOSFET input stage; a transistor in the amplifier's feedback loop provides the requisite logarithmic output, and a diode-transistor combination inserted in the feedback loop provides temperature compensation for the logarithmic feedback element.

The circuit operates as follows: The emitter voltage of Q1 is related logarithmically to the photodiode current; with operational amplifiers of high input impedance, the photocurrent is identical to the current in the feedback element. Since the cathode of the photodiode is near ground, its anode is held at approximately this voltage by the operational amplifier; thus the photodiode is held at a potential near zero bias. Moreover, the collector-base diode of Q1 must also be operated near zero bias to

minimize leakage current in this element and to extend its logarithmic response at low current levels. The temperature coefficients of Q2 and CR1 are similar to those of Q1; to oppose and cancel base-emitter temperature variations in Q1, the circuit elements R1, R2, CR1, and Q2 are arranged as shown in the diagram. The ratio of R1 and R2 establishes the net effective temperature coefficients of the combination of CR1 and Q2 to match that of Q1.

The output voltage obtainable from Q1 is limited to about 0.5 V (an inherent property of silicon semiconductors), but the additional gain is obtained by the ratio of (R4 + R12) to R5. The zero control segment of the circuit permits adjustment of zero conditions by applying a small voltage to the R5 terminal that ordinarily would be grounded.

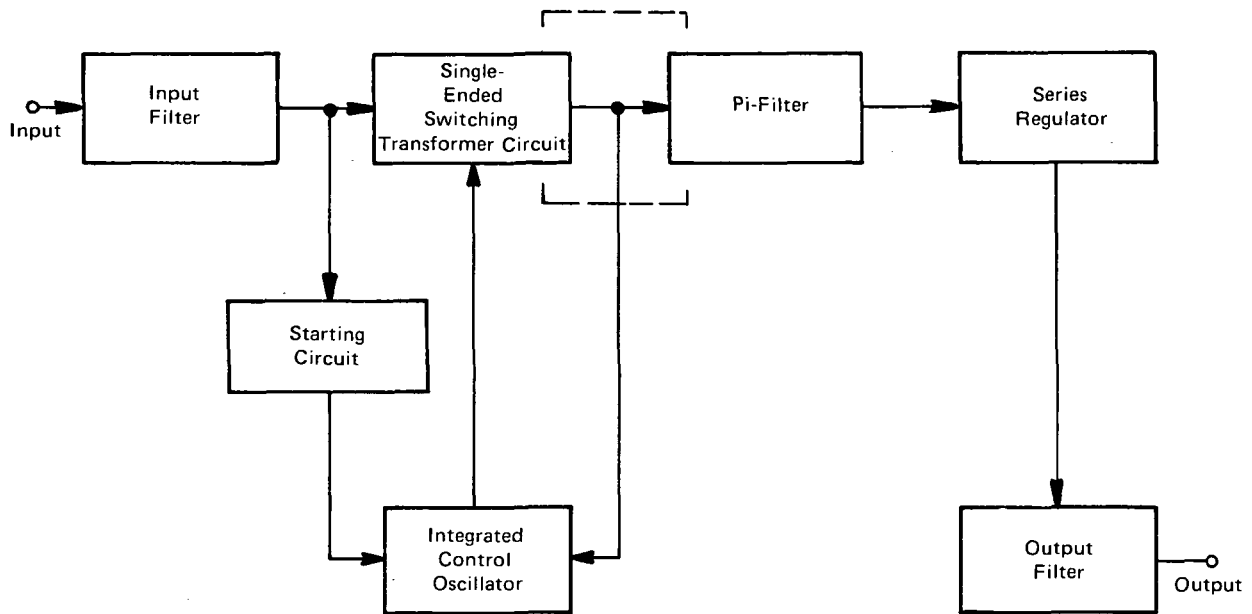
Additional temperature compensation is provided by thermistor R12 and the voltage divider R11 which reduces the residual bias across the photodiode and thereby reduces its temperature-sensitive leakage current.

The radiometer has a $\pm 10\%$ reading accuracy throughout the 5-decade dynamic range while operating over a temperature interval of 0° to 45° C. The output noise of the radiometer is less than 20 millivolts at 10^{-9} watt, and operation at frequencies down to dc is therefore possible; however, the decay response is such that about a tenth of a second is required for the output to become zero in complete darkness. The frequency response is limited by C1, C2, and the effective resistance of Q1.

Source: C. N. Burrous, E. E. Whiting,
Gordon J. Deboo, and William A. Page
Ames Research Center
(ARC-10287)

Circle 11 on Reader Service Card.

SOLID STATE SINGLE-ENDED SWITCHING DC-to-DC CONVERTER



In many circuit applications, a dc supply is required to be electrically isolated from the prime dc power source. Such isolation is normally obtained by means of a dc-to-dc converter involving several stages consisting of rather complex circuitry.

This solid state, single-ended switching dc-to-dc converter provides a highly regulated, electrically isolated dc output voltage with only one power stage.

The converter may be divided into seven distinct subcircuits as illustrated in the block diagram. The series regulator is required only where precise regulation must be had. The input and output filters are included specifically to enhance the electromagnetic compatibility of the converter and thus meet rather stringent radio frequency interference requirements.

The starting circuit performs two functions: it assures that the on time of its output transistor is of sufficient duration to start the integrated control oscillator at the lower temperature limit of -20°C ; and it assures that the off time is long compared to the on time of the power transistor in the single-ended switching transformer circuit. In the integrated control oscillator, an astable multivibrator coupled with an integrated high performance operational am-

plifier, is used to control the operating frequency of the converter, and thus, to regulate the output voltage.

Output voltage ripple associated with the converter storage capacitor is partially controlled by selecting a capacitor with a low dissipation factor and further decreased by adding an inductive-capacitive Pi-filter to this circuitry. The series regulator is designed to provide the desired regulation although a slight decrease in overall converter efficiency results from its use. It provides a high frequency cutoff and a decreased output impedance at the higher operating frequencies.

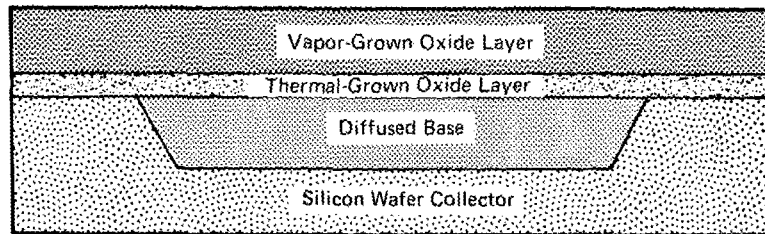
Output voltage is within $\pm 0.325\%$ of the nominal 28 vdc output voltage over the complete design temperature, load, and input voltage ranges. The converter has a maximum dc output impedance of $0.1021\ \Omega$ and maintains an overall efficiency of approximately 80% under all operating conditions.

Source: M. A. Honnell of
Auburn University
under contract to
Marshall Space Flight Center
(MFS-13598)

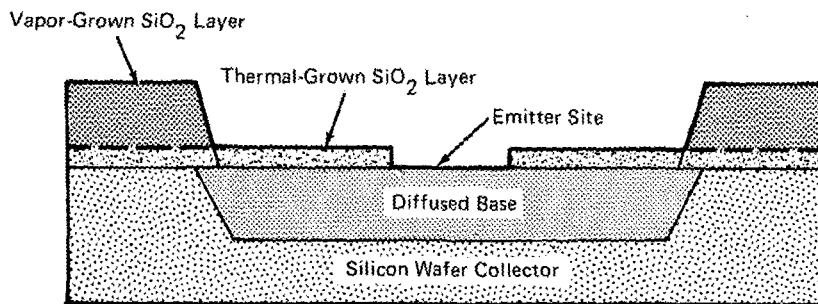
Circle 12 on Reader Service Card.

Section 3. Processes and Techniques for Improving Solid State Devices

VAPOR GROWN SILICON DIOXIDE IMPROVES TRANSISTOR BASE-COLLECTOR JUNCTIONS



BASIC CONFIGURATION



FINAL CONFIGURATION

The thermally grown SiO₂ layer normally used to mask the face of the transistor is extremely thin and may have imperfections that could allow the diffusion of impurities into the silicon wafer in the critical junction region.

A vapor grown SiO₂ layer covers the entire base-collector junction region. This provides an oxide of greater thickness than can be grown compatible with diffusion times and temperatures and fills in any imperfections that exist in the thermally grown layer.

A portion of the thermally grown SiO₂ layer is selectively removed from the face of the silicon wafer by photoengraving. The base region is then diffused into the silicon wafer and a second thermally grown SiO₂ layer is deposited over the entire face of the assembly. The vapor grown SiO₂ layer is now formed by a chemical reaction with silane (SiH₄) and oxygen at a temperature between 422 and 589 K (300° and 600° F). Any imperfections that may have existed in the thermally grown layer are filled by the vapor grown layer. The emitter site is next prepared by removal of appropriate portions of the vapor grown

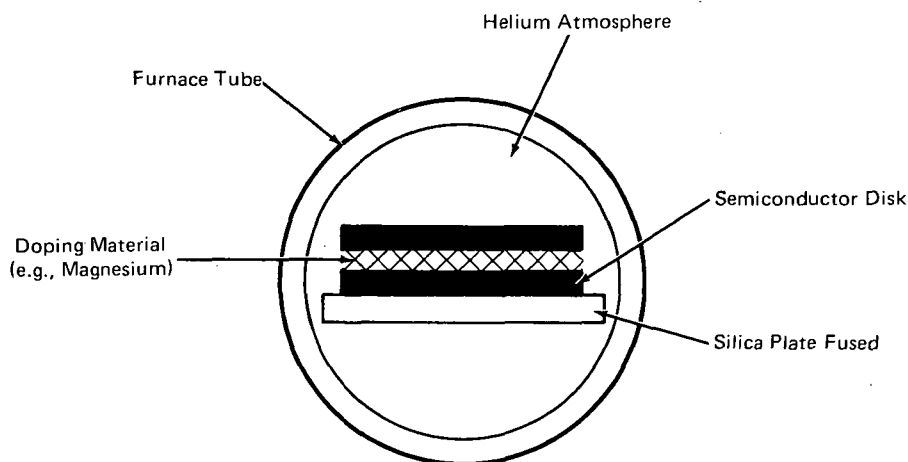
and thermally grown dioxide to expose the diffused base region. The vapor grown oxide covers imperfections that may exist in the layer of thermally grown oxide in the collector-base region and also prevents penetration to the silicon surface, in critical regions of the junction, of imperfections normally formed during photoengraving of emitter sites. All of the collector-base junction is adequately covered with oxide to prevent penetration of phosphorous during the subsequent emitter diffusion step.

In laboratory tests, devices prepared by this process were able to deliver 50% efficiency at more than 20 watts of power and a frequency of 430 MHz. Prior devices are limited to 5 watts at such high frequency. This process could be used to deposit protective SiO₂ coatings on optical surfaces.

Source: R. A. Duclos and D. R. Carley of
Radio Corporation of America
under contract to
Goddard Space Flight Center
(GSC-389)

Circle 13 on Reader Service Card.

TECHNIQUE FOR DOPING SEMICONDUCTOR MATERIALS



Schematic of Furnace and Semiconductor "Sandwich" Used to Dope Materials With Low Diffusion Coefficients

This technique introduces into bulk semiconductor material, elements that have low diffusion coefficients or low solubilities and which are highly reactive. Mainly, the technique employs containment of the doping elements in a sandwich of semiconductor material to inhibit evaporation during the period of high temperature required for diffusion.

The illustration shows the general technique. Two disks of the semiconductor material are plated with thin films of the desired impurity and placed together to form a sandwich. Only a negligible portion of the impurity surface is exposed to other than the semiconductor material. The sandwich is placed on a flat tray of fused silica and the assembly is put in a tube furnace that has been purged with helium. A continuous flow of helium provides a slight positive pressure which is maintained throughout the heat cycle.

A moderate temperature is maintained at the beginning of the process and, after a short interval, the assembly may be raised to any temperature below

the melting point of the semiconductor material. The furnace is cooled in slow steps after the process is completed, in order to prevent cracking of the material.

Some low diffusion coefficient materials may require a double deck sandwich, in which case both sides of the center wafer and the contacting faces of the top and bottom wafers would be vapor plated. Upon completion of the process, the top and bottom wafers are ground off.

This procedure has been used successfully for doping silicon with magnesium, beryllium, and lithium. For example, a heat cycle of 1623 K (1350° C) for 30 minutes provided a Mg concentration of 5×10^{14} atoms/cc.

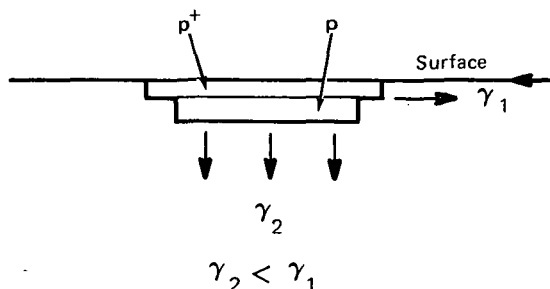
Source: M. F. McNear
Langley Research Center
(LAR-10133)

Circle 14 on Reader Service Card.

DOUBLE-DIFFUSED EMITTER FOR LATERAL PNP TRANSISTORS

A lateral pnp transistor, to be useful, should have a current gain at least 100:1 higher than the parasitic action to the substrate. A double-diffused emitter should result in a lower injection efficiency in the vertical direction than in the lateral direction. The figure demonstrates the action discussed.

The diffusion used for the base and resistor regions of the standard npn-IC is now diffused beneath the lateral pnp emitter. It has been experimentally determined that both the lateral and vertical pnp current gains are lower for a 200 ohms emitter diffusion. Now the regular p^+ emitter diffusion is placed above the base diffusion and extended laterally beyond it. The injection efficiency of the p^+ region extending beyond the p region is higher. Lateral pnp action is not actually improved, but rather vertical action is inhibited. This is important, for, if the lateral action is sufficient, but the vertical action is not less by 100:1, usefulness of the device is considerably limited.



Source: R. C. Gallagher and J. M. Scott of
Westinghouse Electric Corp.
under contract to
Johnson Space Center
(MSC-13089)

No further documentation is available.

ALUMINUM DOPING IMPROVES SILICON SOLAR CELLS

A shallow-junction solar cell having a broad spectral response, high efficiency, and a long lifetime in nuclear radiation environments has been constructed.

It is an aluminum-doped silicon solar cell with resistivities in the 10- to 20-ohm-centimeter range.

The cell is made by a standard diffusion process at temperatures of approximately 800°C, using a high-purity aluminum-doped silicon. The sheet resistance of the diffused layer is kept at or below 200 ohms per square, and 10 grid fingers on the top surface of the cell permit attainment of curve power factors of 70% for this value of sheet resistance. Depending on the application, the cell thickness can vary between 0.002 and 0.050 cm (0.008 and 0.020 inch). A special, antireflective superblue coating increases spectral response which increases resistance to radiation damage.

Application advantages of these cells are: (1) extremely shallow junctions with improved junction

characteristics, resulting in better curve power factors, broader spectral response, and higher efficiencies; and (2) relatively high resistance to nuclear radiation damage. Production advantages of these cells are: (1) low material rejection and increased production yields; (2) close-tolerance control; and (3) ease of applying superblue coatings to improve the spectral response and radiation resistance of the cells.

The following documentation may be obtained from:
National Technical Information Service
Springfield, Virginia 22151
Single document price \$3.00
(or microfiche \$0.95)

Reference:

NASA-TN-D-2711 (N65-18215) Effects of Impurities on Radiation Damage of Silicon Solar Cells
Source: Lewis Research Center
(LEW-206)

SOLID STATE BISTABLE POWER SWITCH

Various combinations of polyester and metallic materials were investigated in order to provide high current and switching time capabilities for high-current resettable fuses. Intensive testing established that tin and copper demonstrated the best performance for trip current, degree of reliability, and the lowest coefficients of thermal expansion in a group of metals which also included aluminum, zinc, lead, and stainless steel. Tin exhibited excellent switching speeds, stability, and high trip currents.

Early experiments with particle sizes indicated that high currents would cause small particles (~ 325 mesh) to melt and fuse together. In order to decrease the on-resistance and thereby increase the trip current, the total fraction of the metal was greatly increased over that normally used in low current devices. As an alternative, an increase in the area of the particles decreased the resistance per path. Desirable particle sizes varied between 40 and 20 mesh according to the metal and its degree of sphericity.

A commercial silicone-rubber compound was used with metal/matrix ratios, by volume, of 70/30 and 80/20. It was found that silicone compounds possessed low viscosity, produced residues, and had approximately the same coefficient of thermal expansion and dielectric as polyester. The silicone-rubber compound was used without a catalyst which produced a consistency more similar to a paste than a rubber. The addition of a catalyst produced failures of the testing device after the first trip.

The first trials of silicone compounds were unsuccessful because high voltages (~ 500 V) were required for reset and trip currents were low. It was shown that an increase in metal content up to a 90/10 ratio would allow a device to carry a 25-amp load for several seconds before tripping.

Electrode size and separation was investigated and found to be significant in performance of electrical devices. A comparison of circular copper electrodes with 7.1 and 12.7 mm (5/16-in. and 0.5-in.) diameter indicated a reduction in width-at-half-maximum of the distribution of trip currents. Separation distances of 100 mils, 150 mils, and 200 mils, average trip currents of 9, 7, and 5 amps, and reset voltages greater than 50 for the first two conditions and less than 100 for the last were tested in combination. It was shown that on-resistance varied inversely as trip current. The inverse dependence of trip current on electrode separation was also consistent with the same general rule. Devices with larger separations required higher reset voltages.

Although a previous study had demonstrated that low-current silicone-rubber devices can be cycled 30,000 times without failure, the current program had problems in device performance during extended cycling (tripping and resetting). It was found that encapsulation of the high current device was a fault. Much of the difficulty was eliminated when the expansion and contraction of tubing was controlled.

The following documentation may be obtained from:

National Technical Information Service
Springfield, Virginia 22151
Single document price \$6.00
(or microfiche \$0.95)

Reference:

NASA-CR-86103 (N68-35634), Solid State Bistable Power Switch Study

Source: H. Shulman and J. Bartko of
Isotopes Inc.
under contract to
Electronics Research Center
(ERC-10290).

CHEMICAL REGENERATION OF EMITTER SURFACE INCREASES THERMIONIC DIODE LIFE

Thermionic diodes produce electrical power directly from heat energy by thermionic emission. The diodes' operating efficiency increases with the operating temperature of the emitter electrode. At high operating temperatures, however, sublimation of the emitter material can destroy the structural integrity

of the emitter and collector surfaces or cause a short between these surfaces.

Regeneration of the emitter electrode can be achieved by chemical transport reactions. A gas that will form chemical compounds with the sublimated emitter material is introduced into the space between

the emitter and the collector. The compounds migrate to the emitter where they decompose and redeposit the emitter material.

Experimentation using a simulated thermionic diode, incorporating a tungsten emitter and a tungsten collector, with chlorine gas introduced as the chemical transporting agent, has shown that emitter regeneration occurs at chlorine partial pressures of 10^{-4} torr and higher, and at emitter temperatures of 2170 to 2550 K and collector temperatures of 1460 to 1730 K. These results indicate that the regenerative process is applicable over the range of pressures and temperatures generally encountered in thermionic diodes.

Although regeneration of hot metallic surfaces by chemical transport has been used to extend the life

of incandescent and photoflood lamps, the process has not previously been applied to thermionic diodes.

The following documentation may be obtained from:

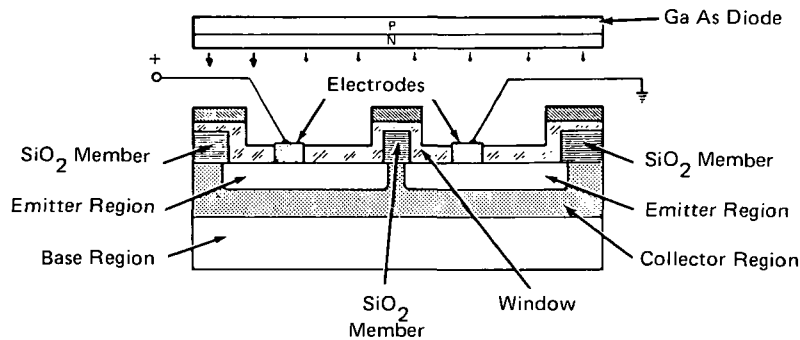
National Technical Information Service
Springfield, Virginia 22151
Single document price \$6.00
(or microfiche \$0.95)

Reference:

NASA-TN-D-1877 (N63-18662) Experimental Investigation of Chemical Regeneration of Surfaces in Simulated Thermionic Diodes

Source: R. Breitwieser
Lewis Research Center
(LEW-17)

OPAQUE COATINGS REDUCE TURN-OFF TIME OF OPTICALLY-DRIVEN SWITCH



To reduce the turn-off response time of an optically driven silicon switch, place an opaque covering over the passivating silicon dioxide members to prevent photon absorption. Turn-off time of the switch is lengthened by the absorption of photons, by the passivating silicon dioxide members, which causes carriers to be trapped or stored in the base region.

The switch includes a pair of space planar emitter regions set in a base region formed above a collector region. Passivating silicon dioxide members cover those portions of the emitter-base junctions that extend to the upper semiconductor surface. Windows of a suitable transparent material cover the upper surfaces of the emitter regions. Only two small portions that serve as the input and output electrodes of the switch are not covered by the windows.

When a suitable light source, such as a forward biased gallium arsenide diode, illuminates the upper

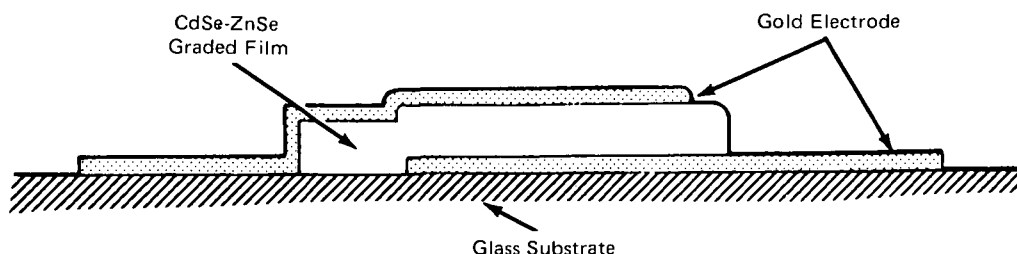
surface of the normally off silicon switch, an electrical circuit is established between the two emitter regions. Removal of the light turns the switch off.

The use of an opaque coating over the silicon dioxide prevents photon absorption so that carriers are not trapped or stored in the surface of the base region, thus materially shortening turn-off response. In the absence of an opaque coating, the turn-off time for the silicon switch is longer than desired for some purposes, being as great as a few milliseconds. When an opaque coating is used, response times on the order of 80 microseconds may be obtained.

Source: IBM Corp.
under contract to
Jet Propulsion Laboratory
(JPL-SC-107)

Circle 15 on Reader Service Card.

THIN-FILM SEMICONDUCTOR RECTIFIER HAS IMPROVED PROPERTIES



A cadmium selenide (CdSe)-zinc selenide (ZnSe) film, vapor-deposited in a controlled concentration gradient onto a glass substrate forms the required junctions between vapor-deposited gold electrodes to provide an improved thin-film semiconductor rectifier.

The relative proportions of CdSe and ZnSe along the thickness of the semiconductor film are varied by controlling the vapor-deposition process. In this manner, the CdSe concentration will be greater at one boundary than at the other boundary of the semiconductor film where junctions are formed with the vapor-deposited gold emitter and collector electrodes. The junction between the CdSe-rich portion of the semiconductor film and one gold electrode will present a relatively low energy barrier, whereas the junction between the ZnSe-rich portion of the semiconductor film and the other gold electrode will present a relatively large energy barrier.

The magnitude of the larger energy barrier, which primarily determines the current that can be passed through the rectifier, can be varied by an applied potential to produce an asymmetrical current-voltage characteristic. The relationship between the log of

the current and the square root of the voltage is linear up to a voltage determined by the ZnSe-rich boundary.

Tests on rectifier samples (0.058 cm² in area) made by this procedure yielded the following results:

Static rectification ratio at 0.4 volt	10 ⁵
Forward resistance	100 ohms
Reverse breakdown potential	7 volts
Forward breakdown potential	0.3 volt
Leakage current at 4 volts reverse bias	less than 1 microamp
Maximum forward current density	2 amp/cm ²
Shelf life (room temperature)	2000 hours

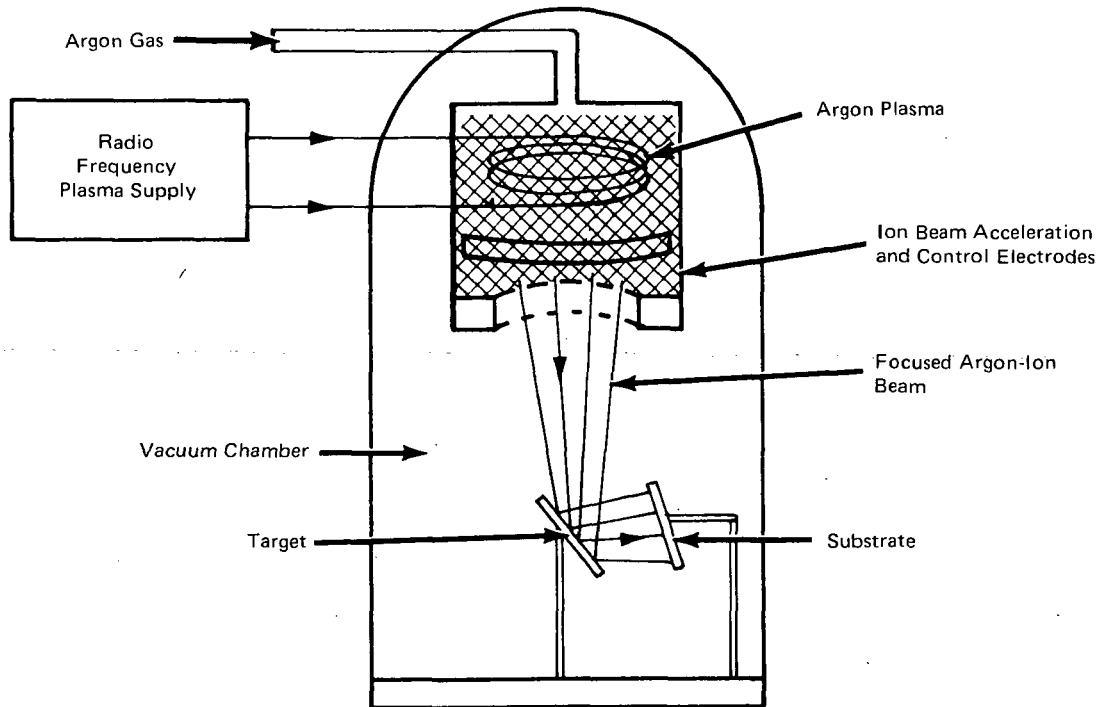
Title to this invention, covered by U. S. Patent No. 3,441,429, has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)] to Melpar, Inc., Falls Church, Virginia 22046.

Source: Melpar, Inc.,
under contract to
Johnson Space Center
(MSC-207)

EPITAXIAL CRYSTALLINE GROWTH ON COLD SUBSTRATES

A method of growing thin films epitaxially on cold substrates has been developed. It was discovered that, by sputtering a material with a high-energy ion-beam bombardment, the molecules of the target's substance can be dislodged and ejected for subsequent deposition on a cold substrate of the desired crystallographic type and orientation. The orientation of the condensate to some finite thickness is controlled epitaxially by the substrate.

The pertinent features of this method are shown in the accompanying figure. A shaped argon ion beam, having a density of about 1 mA/cm² and energy up to 5 keV, is directed on a target material to be sputtered. The ejected material from the target is then collected on a suitable substrate located outside the immediate path of the ion beam. The temperature of the substrate is that of the ambient temperature of the vacuum chamber (approximately 75° C). In this



specific experiment crystalline olivine (Mg_2SiO_4) is used as the target material, and the collection of the condensate is made upon a substrate of salt (NaCl) crystal. A layer of film $100\ \mu$ thick is deposited in one hour. An examination of the thin film with an electron microscope reveals that it is slightly crystalline, and could be identified as belonging to either the isometric or hexagonal crystal system. Since the olivine target is crystallographically in the orthorhombic system, it is evident that a new material is deposited.

In the past, epitaxial growth has been achieved by collecting condensates on substrates having elevated temperatures of about 523 K or higher. In this process thermal energy has been employed to produce condensates by evaporating and subsequently condensing materials on selected substrates. This energy provides the molecular mobility needed for crystal growth and orientation. In the instant method, how-

ever, the molecules sputtered from the target have kinetic energies of from 3 to 20 eV, in contrast to the thermal energies of about 0.1 eV in the case of the previously mentioned evaporants. This higher energy provides the needed mobility and assists in the epitaxial growth on the substrate. Although the principal advantage of this method initially appears to be the elimination of substrate heaters, it is likely that the production of epitaxial thin films having superior electrical and physical properties will be possible through its application.

Source: R. L. Lebduska of
Physics Technology Laboratories, Inc.
under contract to
Johnson Space Center
(MSC-11196)

No further documentation is available.

TECHNIQUE FOR PRODUCING BIPOLAR AND MOS FIELD EFFECT TRANSISTORS ON A SINGLE CHIP

A method has been described for the simultaneous production on a single, monolithic silicon chip of vertical npn transistors, lateral pnp transistors, and p-channel, enhancement mode MOSFET devices.

Initially, two epitaxial layers are grown on a p-type silicon substrate. The first, p-type, is heavily doped with arsenic, and the second, n-type, is heavily doped with phosphorus. After the surface layer is oxidized, several cycles follow of photoetching, dopant deposition, and drive-in, to produce selectively-doped regions and semiconductor junctions within the chip. In the first cycle, the areas exposed by photoetching are heavily doped with boron. These p-type regions, together with the p-type arsenic doped epitaxial substrate, form channels which isolate each device from its neighbors. Second, the base region of the npn transistor is doped with boron and driven in deeply, to leave space for the emitter. Third, the emitter and collector of the lateral pnp transistor, and the source and drain of the MOSFET are doped with boron. Fourth, the npn emitter and the pnp base are doped with phosphorus.

Next, the gate region of the FET is exposed, the device is thoroughly cleaned, and the gate dielectric

is oxidized. The dielectric is then doped with phosphorus, which at the same time forms a phosphorus glass passivation layer over the entire chip.

Immediately following the doping of the dielectric, a layer of aluminum is deposited over the entire chip by electron beam evaporation. This layer prevents shorts through the dielectric and protects it from contamination.

Contact windows are etched through the aluminum and through the underlying oxide, and a second layer of aluminum is deposited, filling the contact windows. Subsequently, a final etching separates the contact regions and forms the bonding pads and interconnections. After sintering to form ohmic contacts, the wafers are ready for final evaluation, scribe and dice, and packaging.

Source: D. W. Williams and
R. C. Gallagher of
Westinghouse Electric Corp.
under contract to
Johnson Space Center
(MSC-13358)

No further documentation is available.

Section 4. Radiation Effects on Solid State Devices

ION IMPLANTATION REDUCES RADIATION SENSITIVITY OF METAL-OXIDE-SILICON (MOS) DEVICES

In MOS devices, ionizing radiation produces two effects on thermally grown silicon oxide on silicon: (1) a net positive space charge is created in the oxide; and (2) fast surface states are introduced at the oxide/silicon interface. Both of these effects can produce structural instabilities in metal-oxide-silicon devices, and can cause circuits that are operating satisfactorily to drift and malfunction.

The implantation of N_2 ions, however, can be used to harden the silicon oxide against the effects of ionizing radiation.

Two changes in silicon oxide contribute to radiation hardening: (1) the introduction of impurities to perturb electronic levels, altering carrier kinetics; and (2) the formation of structural imperfections. Both of these are accomplished by the technique of ion implantation. The properties of a standard, thermally grown silicon oxide are modified, reducing the sensitivity to ionizing radiation, yet preserving the stability normally shown by interfaces between silicon and thermally grown oxides.

For implantation, an ion source was used to generate a nitrogen ion plasma. Ions were extracted from this plasma and then accelerated down a 61 to 91 cm (2 to 3 ft) column by a 6.4×10^{14} J (400 keV) Van de Graaff accelerator. A beam of N_2^+ ions was then isolated by an analyzing magnet capable of sorting ions into species of specific mass-to-charge ratios. A quad magnet was used to spread the beam, improving the beam pattern uniformity ($\pm 30\%$ of nominal). Successful implantations were carried out with 8.10×10^{15} J (50 keV) N_2^+ particles at a flux rate of $10^{16}/\text{cm}^2$.

The target chamber was evacuated to about 1.33 MN/m^2 (10^5 torr) by an oil-free turbomolecular pump. The temperature of the targets was held within a range of about 283 to 288 K above room temperature. The targets themselves were standard, thermally grown silicon oxide, 2000 Å thick, on silicon.

The chief source of irradiation throughout the experiment was a Brad-Thompson electron gun. Electron energies varied from 6.4×10^{16} to 3.2×10^{15} J (4 to 20 keV), with 3.2×10^{15} J being used for most of the irradiations, and the flux varying from 10^{12} to 10^{17} particles/ cm^2 .

The primary property measured in analyzing the oxides and modified oxides was the capacitance-voltage property of a metal-oxide-silicon structure. While the method is extremely powerful for understanding the properties of the oxide-silicon interface, the only quantitative value recorded during these experiments was that of the flat-band voltage. This is the voltage, applied to the metal electrode, at which the MOS capacitor has the capacitance value corresponding to zero potential applied to the ideal capacitor. (The ideal capacitor is a capacitor in which all voltages applied to the metal electrode are balanced by charges in the silicon surface space-charge region). Consequently, the flat-band voltage is a measure of departure from the ideal capacitance.

In these experiments, it was assumed that the change in the flat-band voltage value was an effect caused by charges introduced during irradiation. These charges could either be in the form of an oxide space-charge or an interface state at the oxide/silicon interface. The flat-band value does not distinguish between these two charge sources.

The experiments showed that the radiation hardness of thermal oxides improved 30% to 60% as a result of N_2^+ ion implantation. This approach to radiation hardening retains all the advantages of the well-established and highly perfected techniques of thermal oxidation, and requires the degradation of only one specific property: the electron lifetime in the oxide. Most of the work of this investigation was carried out on implantations which were sufficiently high in fluence to introduce a small shift in the initial capacitance-voltage characteristic of the MOS device used for evaluating the modification. The magnitude of this shift is small compared to the improvement in radiation hardness, but does vary with fluence. The optimum ion, fluence, and range (energy) have not yet been identified.

The following documentation may be obtained from:
National Technical Information Service
Springfield, Virginia 22151
Single document price \$3.00
(or microfiche \$0.95)

Reference:
NASA-CR-1584 (N70-26555), The Development of Radiation Resistant Insulating Layers for Planar Silicon Technology.

Source: Research Triangle Institute
under contract to
Langley Research Center
(LAR-10630)

EFFECTS OF IONIZING RADIATION ON TRANSISTOR SURFACES

While it is generally known that a low energy X-ray generator produces ionizing radiation surface effects in silicon planar devices and that high-temperature anneals surface damage, the concept of using both sequentially as a screening technique has not been reported heretofore. The screening test technique employs an ionizing radiation field in which electrically-biased devices are placed for a time long enough to produce changes in surface properties that are large enough to be easily observed. In this study, the radiation field was generated by an X-ray generator, and the electrical bias producing the greatest changes in bipolar transistors was a reverse-biased collector-base junction. For field effect transistors, biases that normally cause the device to be cut off are used. Small amounts of radiation exposure (about 10^5 R) produce large changes in the surface properties when the devices are biased as described.

After radiation, common emitter current gain h_{FE} at low values of collector current and collector leakage current I_{CBO} data are used to determine which bipolar transistors have poor surfaces. Similar surface-sensitive electrical parameters can be chosen to evaluate other device types. The transistors with poor surfaces exhibit large, rapid decreases in h_{FE} and large values of I_{CBO} that can be several orders of magnitude greater than that observed in other devices of the same type with good surface characteristics. The good devices are then annealed to pre-irradiation conditions.

The screening test is a tool for the design engineer, since it provides design information concerning the electrical characteristics of transistors,

and hence the circuit that is exposed to ionizing radiation environments. This is of particular interest to those who are concerned with space radiation effects, weapon environments, reactor environments, and nuclear propelled vehicles.

Of equal importance is the implication that non-irradiation quality-assurance programs can be enhanced, because the screening technique reveals those devices that have poor surface properties. With such a tool, devices with poor surface properties can be eliminated for both irradiation and non-irradiation environments where high reliability is a concerning factor. This is an important consideration because the surface instabilities are vulnerable to high temperature as well as radiation environments.

The radiation portion of the screening procedure is not restricted to the use of an X-ray generator but can use any ionizing source which does not cause bulk damage. It may be possible for device manufacturers to perform efficient screening programs on the assembly-line before the semiconductor material is encapsulated, using an electron source of ionizing radiation.

This screening technique is effective for SiO_2 passivated planar structures; it was not effective on alloy junction or mesa structures.

Source: R. J. Sweet and D. L. Nelson of
Bendix Corp.
under contract to
Marshall Space Flight Center
(MFS-13818)

Circle 16 on Reader Service Card.

Patent Information

The following innovations, described in this Compilation, have been patented or are being considered for patent action as indicated below.

Silicon Carbide Diode for Increased Light Output (Page 3) MFS-20063

Title to this invention, covered by U.S. Patent No. 3,205,101, has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to: Tyco Laboratories, Inc., Bear Hill, Waltham, Massachusetts.

Hybrid Solid State Switch Replaces Motor-Driven Power Switch (Page 9) JPL-931

This invention has been patented by NASA (U.S. Patent No. 3,430,063). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
NASA Pasadena Office
Mail Code I
4800 Oak Grove Drive
Pasadena, California 91103

Fused Diode Provides Visual Indication of Fuse Condition (Page 12) KSC-67-16

This invention has been patented by NASA (U.S. Patent No. 3,340,430). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Kennedy Space Center
Code AD-PAT
Kennedy Space Center, Florida 32899

RF Noise Suppression Using the Photodielectric Effect in Semiconductors (Page 13) MSC-12259

This is the invention of a NASA employee, and U.S. Patent No. 3,694,753 has been issued to him. Inquiries concerning license for its commercial development may be addressed to the inventor: Mr. G. D. Arndt, Lyndon B. Johnson Space Center, Code EE8, Houston, Texas 77058.

Solid State Variable Time Delay (Page 14) ERC-10032

This invention has been patented by NASA (U.S. Patent No. 3,568,103). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
NASA Headquarters
Code GP
Washington, D. C. 20546

Semiconductor Forms Biomedical Radiation Probe (Page 15) MSC-320

This invention has been patented by NASA (U.S. Patent No. 3,427,454). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to:

Patent Counsel
Lyndon B. Johnson Space Center
Code AM
Houston, Texas 77058

Thin-Film Semiconductor Rectifier Has Improved Properties (Page 24) MSC-207

Title to this invention, covered by U.S. Patent No. 3,441,429, has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to: Melpar, Inc., Falls Church, Virginia 22046.



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